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[METHOD FOR OPTIMAL USE OF DIRECT FIT AND INTERPOLATED MODELS IN SCHEMATIC CUSTOM DESIGN OF ELECTRICAL CIRCUITS]

Abstract

A method of analyzing and designing circuits comprising creating a set of interpolated models for transistor devices; creating a set of characterized (direct fit) models for the transistor devices; analyzing the transistor devices within a netlist for matches in the set of characterized models; and providing a choice of using the matched characterized models or one of the interpolated models in designing the circuits. The method further comprises schematically simulating a custom circuit; back annotating to a schematic circuit which of the transistors use direct-fit models and which of the transistor devices are interpolated; determining whether the transistor devices are in any of cutoff, saturation, static linear, and dynamic linear mode during simulation of the custom circuit; removing the saturation and dynamic linear mode transistor devices; back annotating the netlist to a schematic with a predeter-

mined device state; and performing sensitivity analysis on saturation and dynamic linear mode transistor devices.